CLAIMS

What is claimed is:

1. A method of signal processing, comprising:

converting an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal;

sampling the electrical signal using two or more sampling windows to generate two or more bit estimate values; and

applying a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal.

2. The method of claim 1, wherein the two or more sampling windows correspond to a single signaling interval.

3. The method of claim 1, wherein:

each sampling window has a width;

the electrical signal has a series of waveforms comprising first and second pluralities of waveforms, wherein each waveform of the first plurality represents a binary "0" and each waveform of the second plurality represents a binary "1"; and

for each sampling window:

a waveform is integrated over the sampling window width to generate a corresponding bit estimate value; and

the sampling window width is selected to reduce contribution of the second plurality of waveforms into integration results corresponding to the first plurality of waveforms.

4. The method of claim 1, wherein:

sampling the electrical signal comprises:

integrating the electrical signal over a first sampling window to generate a first integration result;

comparing the first integration result with a first decision threshold value to generate a first bit estimate value;

integrating the electrical signal over a second sampling window to generate a second integration result; and

comparing the second integration result with a second decision threshold value to generate a second bit estimate value; and

applying the logical function comprises applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

5. The method of claim 4, wherein the first decision threshold value is different from the second decision threshold value.

6. The method of claim 1, wherein the optical signal is an optical duobinary signal.

7. The method of claim 1, comprising:

generating a first clock signal based on the electrical signal;

multiplying a frequency of the first clock signal to generate a second clock signal; and

sampling the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying first and second bit estimate values.

8. The method of claim 7, comprising:

separating the first and second bit estimate values from the bit stream while discarding all other bits of the bit stream; and

applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

9. The method of claim 1, comprising:

generating a clock signal based on the electrical signal;

sampling first and second copies of the electrical signal at a sampling rate corresponding to the clock signal, wherein:

the first copy is sampled to generate a first bit estimate value;

the second copy is sampled to generate a second bit estimate value; and

the first and second copies are sampled with a relative time delay.

10. The method of claim 9, comprising applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

11. An optical receiver, comprising:

a signal converter adapted to convert an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal; and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows to generate two or more bit estimate values; and

(ii) apply a logical function to the two or more bit estimate values to generate a bit

sequence corresponding to the optical signal.

12. The receiver of claim 11, wherein the two or more sampling windows correspond to a single signaling interval.

13. The receiver of claim 11, wherein the optical signal is an optical duobinary signal.

14. The receiver of claim 11, comprising:

a decision circuit coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal; and

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal, wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying first and second bit estimate values.

15. The receiver of claim 14, comprising:

a de-multiplexer having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit;

a first output port is adapted to receive a signal corresponding to the first bit estimate value; and

a second output port is adapted to receive a signal corresponding to the second bit estimate value; and

an "AND" gate coupled to the first and second output ports and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

16. The receiver of claim 11, comprising:

first and second decision circuits, each coupled to the signal converter;

a clock recovery circuit coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal;

the first decision circuit is adapted to generate a first bit estimate value;

the second decision circuit is adapted to generate a second bit estimate value; and

the first and second decision circuits sample the electrical signal with a relative time delay.

17. The receiver of claim 16, comprising an "AND" gate coupled to the first and second decision circuits and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

18. The receiver of claim 16, wherein each decision circuit is adapted to:

integrate the electrical signal over a sampling window to generate an integration result; and

compare the integration result with a decision threshold value to generate a bit estimate value.

19. The receiver of claim 18, wherein the first and second decision circuits use different decision threshold values.

20. An optical communication system, comprising an optical receiver coupled to an optical transmitter via a transmission link, wherein the optical receiver comprises:

a signal converter adapted to convert an optical signal into an electrical signal having an amplitude corresponding to optical power of the optical signal; and

a decoder coupled to the signal converter and adapted to:

(i) sample the electrical signal using two or more sampling windows to generate two or more bit estimate values; and

(ii) apply a logical function to the two or more bit estimate values to generate a bit sequence corresponding to the optical signal.

21. The system of claim 20, wherein the two or more sampling windows correspond to a single signaling interval.

22. The system of claim 20, wherein the optical signal is an optical duobinary signal.

23. The system of claim 20, wherein the optical receiver comprises:

a decision circuit coupled to the signal converter;

a clock recovery circuit coupled to the signal converter and adapted to generate a first clock signal based on the electrical signal;

a clock multiplier coupled between the clock recovery circuit and the decision circuit and adapted to multiply a frequency of the first clock signal to generate a second clock signal, wherein the decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the second clock signal to generate a bit stream carrying first and second bit estimate values;

a de-multiplexer having an input port and a plurality of output ports, wherein:

the input port is coupled to the decision circuit;

a first output port is adapted to receive a signal corresponding to the first bit estimate value; and

a second output port is adapted to receive a signal corresponding to the second bit estimate value; and

an "AND" gate coupled to the first and second output ports and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

24. The system of claim 20, wherein the optical receiver comprises:

first and second decision circuits, each coupled to the signal converter;

a clock recovery circuit coupled between the signal converter and the first and second decision circuits and adapted to generate a clock signal based on the electrical signal, wherein:

each decision circuit is adapted to sample the electrical signal at a sampling rate corresponding to the clock signal;

the first decision circuit is adapted to generate a first bit estimate value;

the second decision circuit is adapted to generate a second bit estimate value; and

the first and second decision circuits sample the electrical signal with a relative time delay; and

an "AND" gate coupled to the first and second decision circuits and adapted to apply an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.